



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,182	10/02/2003	Jee-Soo Mok	LEPA121687	8329

26389 7590 03/08/2006

CHRISTENSEN, O'CONNOR, JOHNSON, KINDNESS, PLLC  
1420 FIFTH AVENUE  
SUITE 2800  
SEATTLE, WA 98101-2347

EXAMINER

AHMED, SHAMIM

ART UNIT PAPER NUMBER

1765

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/677,182	MOK ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Shamim Ahmed	1765	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 10 February 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

**DETAILED ACTION**

***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/10/06 has been entered.

***Response to Arguments***

2. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamayachi et al (4,943,516) in view of Applicant's admitted prior art (AAPA) and further in view of Nakatani et al (US 2002/0026980 A1).

Kamayachi et al disclose a process of forming a solder resist pattern on a printed circuit board (col.1, lines 7-20), wherein the process including the steps of:

- Laminating or depositing a thermosetting resin on a printed circuit board (PCB) having circuits formed thereon, wherein the resin can be in a wet or dry state (semi-cured);
- The coating is then directly exposed to a laser beam through a photomask having a prescribed pattern;
- Post-curing the developed thermosetting resin pattern to form solder resist pattern (col.15, line 67-col.16, line 31).

Kamayachi et al remain silent about the pre-treating the printed circuit board before lamination step.

However, Applicant's admitted prior art (AAPA, herein after) teach pretreating such as scrubbing process is carried out on both sides of the substrate to improve the adhesion between the photo solder resist (PSR) and the substrate (see specification page 6, lines 8-10).

Therefore, it would have been obvious to one of ordinary skilled in the art at the time of claimed invention to combine AAPA's teaching into Kamayachi et al's process

for increasing bonding capability between the circuit board substrate and polymeric solder resist material as taught by AAPA.

Modified Kamayachi et al fail to teach a laser beam is used to produce via hole in the printed circuit board.

However, Nakatani et al disclose a circuit board manufacturing process including the step of forming via holes in the board utilizing drilling, laser beam of Carbon dioxide or excimer laser, wherein laser beam is preferred because of fine precision (paragraph 0087).

Therefore, it would have been obvious to one of ordinary skilled in the art at the time of claimed invention to combine Nakatani et al's teaching into modified Kamayachi et al's process for precisely forming the circuit patterns in the printed circuit board as taught by Nakatani et al.

6. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Urasaki et al (5,879,568) in view of Applicant's admitted prior art (AAPA) and further in view of Nakatani et al (US 2002/0026980 A1).

Urasaki et al wherein the process including the steps of:

- depositing a thermosetting resin on a printed circuit board (PCB) having circuits formed thereon, wherein the resin can be cured by heating (col.2, lines 61-col.3, line 2).
- the resin layer is then selectively irradiating with a laser beam in order to form prescribed solder resist pattern, wherein the types of laser includes

Art Unit: 1765

carbon dioxide laser, YAG laser or excimer laser (col.7, lines 50-58 and col.9, lines 49-col.10, lines 57).

Urasaki et al remain silent about the pre-treating the printed circuit board before lamination step.

However, Applicant's admitted prior art (AAPA, herein after) teach pretreating such as scrubbing process is carried out on both sides of the substrate to improve the adhesion between the photo solder resist (PSR) and the substrate (see specification page 6, lines 8-10).

Therefore, it would have been obvious to one of ordinary skilled in the art at the time of claimed invention to combine AAPA's teaching into Urasaki et al's process for increasing bonding capability between the circuit board substrate and polymeric solder resist material as taught by AAPA.

Modified Urasaki et al fail to teach a laser beam is used to produce via hole in the printed circuit board.

However, Nakatani et al disclose a circuit board manufacturing process including the step of forming via holes in the board utilizing drilling, laser beam of Carbon dioxide or excimer laser, wherein laser beam is preferred because of fine precision (paragraph 0087).

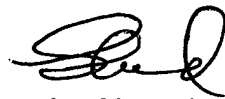
Therefore, it would have been obvious to one of ordinary skilled in the art at the time of claimed invention to combine Nakatani et al's teaching into modified Urasaki et al's process for precisely forming the circuit patterns in the printed circuit board as taught by Nakatani et al.

**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shamim Ahmed whose telephone number is (571) 272-1457. The examiner can normally be reached on M-Thu (7:00-5:30) Every Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Shamim Ahmed  
Primary Examiner  
Art Unit 1765

SA  
March 5, 2006